**3 bit Asynchronous Up counter :**

library IEEE;  
use IEEE.STD\_LOGIC\_1164.ALL;  
  
entity jk\_ff is  
Port ( j : in STD\_LOGIC;  
k : in STD\_LOGIC;  
clock : in STD\_LOGIC;  
reset : in STD\_LOGIC;  
q : out STD\_LOGIC);  
end jk\_ff;  
  
architecture Behavioral of jk\_ff is  
signal jk : std\_logic\_vector(1 downto 0) := "00";  
signal qsig : std\_logic := '0';  
begin  
jk <= j & k;  
process(reset,clock)  
begin  
if (reset = '1')then  
qsig <='0';  
elsif (clock'event and clock = '1')then  
case (jk) is  
when "00" => qsig <= qsig;  
when "01" => qsig <= '0';  
when "10" => qsig <= '1';  
when others => qsig <= not qsig;  
end case;  
end if;  
end process;  
q <= qsig;  
end Behavioral;  
  
**--Step2. VHDL code for 3 bit Counter using structural modeling**  
library IEEE;  
use IEEE.STD\_LOGIC\_1164.ALL;  
  
entity counter\_test is  
Port ( clock : in STD\_LOGIC;  
reset : in STD\_LOGIC;  
count : out STD\_LOGIC\_VECTOR (2 downto 0));  
end counter\_test;  
  
architecture structural\_test of counter\_test is  
  
component jk\_ff is  
Port ( j : in STD\_LOGIC;  
k : in STD\_LOGIC;  
clock : in STD\_LOGIC;  
reset : in STD\_LOGIC;  
q : out STD\_LOGIC);  
end component;  
  
signal temp:std\_logic\_vector(2 downto 0) := "000";  
  
begin  
  
label1 : jk\_ffport map ( reset => reset, clock => clock, j => '1', k => '1', q => temp(2));  
label2 : jk\_ff port map (reset => reset,clock =>NOT temp(2), j => '1', k => '1', q => temp(1));  
label3 : jk\_ff port map ( reset => reset,clock => NOT temp(1), j => '1', k => '1',q => temp(0));  
count(2) <= temp(0);  
count(1) <= temp(1);  
count(0) <= temp(2);  
  
end structural\_test;  
  
--**Step3. Test Bench Code**  
LIBRARY ieee;  
USE ieee.std\_logic\_1164.ALL;  
ENTITY tb\_test1 IS  
END tb\_test1;  
ARCHITECTURE behavior OF tb\_test1 IS  
COMPONENT counter\_test  
PORT(  
clock : IN std\_logic;  
reset : IN std\_logic;  
count : OUT std\_logic\_vector(2 downto 0)  
);  
END COMPONENT;  
--Inputs  
signal clock : std\_logic := '0';  
signal reset : std\_logic := '0';  
--Outputs  
signal count : std\_logic\_vector(2 downto 0);  
BEGIN  
-- Instantiate the Unit Under Test (UUT)  
uut: counter\_test PORT MAP (  
clock => clock,  
reset => reset,  
count => count  
);  
  
process  
begin  
wait for 5ns;  
clock <= not clock;  
end process;  
  
process  
begin  
reset <= '1';  
wait for 50ns;  
reset <= not reset;  
wait;  
end process;  
  
END;